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Application No.	09/827,073	Prepared by	NH	Tracking Number	05914557
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a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
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LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
YOR920000587US1 (13958)	09/827,073

Applicant	
Louis L. Hsu et al.	
Filing Date	**Group**
April 5, 2001	2818

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

TP		"An 8ns Random Cycle Embedded RAM Macro with Dual-Port Interleaved DRAM Architecture (D^2RAM)", Yasuhiro Agata et al, 2000 IEEE International Solid-State Circuits Conference, 9 pages.

EXAMINER	Trong Phan	DATE CONSIDERED	4/9/04

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.